



Physical Sciences Seminar

Gate-based sensing for spin qubits

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The silicon metal-oxide-semiconductor transistor is the workhorse of the microelectronics industry. It is the building block of all major electronic information processing components such as microprocessors, memory chips and telecommunications microcircuits. By shrinking its size generation after generation the computational performance, memory capacity and information processing speed has increased relentlessly. However, the process of miniaturization is bound to reach its fundamental physical limits in the next decades. New computing paradigms are hence paramount to overcome the technical limitations of silicon technology and continue increasing the computation performance beyond simple multi-core approaches. Quantum computing based on computing with interacting two-level quantum systems or qubits- offers exponential speed-up over several classical algorithms [1-3] and it is hence one of the most sought-after alternatives to conventional computing. However, finding the optimal physical system to process quantum information and scale it up to the large number of qubits necessary to run the aforementioned algorithms remains a major challenge. Paradoxically, we are now starting to see that silicon technology itself could offer an optimal platform on which to fabricate spin-based scalable quantum circuits: Quantum computing with silicon transistors fully profits from the most established industrial technology to fabricate large scale integrated circuits while facilitating the integration with conventional electronics for fast data processing of the binary outputs of the quantum processor; all this offering long electron spin coherence times [4]. In this talk, I will present a series of results on fully depleted silicon-on-insulator (FD-SOI) transistors at milliKelvin temperatures that show this technology could provide a platform on to which implement electron-spin qubits [5-10]. Additionally, I will present a set of experiments that demonstrate the potential to scale FD-SOI technology to a large number of qubits and interface them naturally with conventional digital electronics [11-12].

Tuesday, April 10, 2018 11:00am - 12:30pm

Big Seminar room Ground floor / Office Bldg West (I21.EG.101)



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